Abstract - As technology is scaled down, the importance of leakage current and power analysis for memory design is increasing. In this paper, we discover an option for low power interconnect synthesis at the 45nm node and beyond, using Fin-type Field-Effect Transistors (FinFETs) which are a promising substitute for bulk CMOS at the considered gate lengths. We consider a mechanism for improving FinFETs efficiency, called variable-supply voltage schemes. It is well known that leakage savings using transistor stacks is not effective in double-gate technologies such as FinFETs, due to the absence of body effect. However, transistor stacking along with variable supply voltage operation of FinFETs can offer larger leakage savings compared to that of bulk devices. In this paper, we’ve illustrated the design and implementation of FinFET based 4x4 SRAM cell array by means of one bit 7T SRAM. FinFET based 7T SRAM has been designed and analysis have been carried out for leakage current, dynamic power and delay. Furthermore, 2:4 decoder has been designed and results obtained through proposed model have been verified. For the validation of our design approach, output of FinFET SRAM array have been compared with standard CMOS SRAM and significant improvements are obtained in proposed model. 

Keywords - FinFET; 4x4 7T SRAM Cell; leakage current; Delay; Dynamic Power.

1. Introduction

Reduction of power consumption is one of the most important issues in CMOS circuit design. Lowering the supply voltage ($V_{DD}$) is a promising way to reduce power consumption. However, when $V_{DD}$ is lowered, gate delay is increased and hence lower operation frequency. In this paper we use Variable Supply-voltage (VS) scheme that enable $V_{DD}$ reduction without the performance degradation [13,5]. Lower operating voltage is enough to operate SRAM which increases the cell stability. Continuous shrinking of channel length increases the speed of devices in very large scale circuits [12]. This steady miniaturization of transistor with each new generation of bulk CMOS technology has yielded continual improvement in the performance of digital circuits. The scaling of bulk CMOS, however, faces significant challenges in the future due to fundamental material and process technology limits. The 45 nm FINFET based transistors are used for alternative solution for Si-MOSFET with scaled device geometry. In these device structures, the effect of short-channel length can be controlled by limiting the off-state leakage.

In this paper, 16 bit SRAM array using FinFET is proposed. The performance of proposed design is compared among the array using CMOS technology and FinFET. An overview of this paper is organized as follows.

Section 2 shows a FinFET structure, and proposes a FinFET 7T SRAM cell. In section 3, the 16-bit 7T SRAM memory is designed and also the components of array with read/write operation are described. Section 4 describes the voltage variable scheme, and its effects on leakage, dynamic current, and delay. We analyze the comparative CMOS and FinFET array simulation results in section V. The final section draws the conclusions of this work.

2. Background Theory

2.1 Finfet Structure

The continuous down scaling of bulk CMOS creates major issues due to its base material. The primary obstacles to the scaling of bulk CMOS to 32nm gate lengths include short channel effects, Sub-threshold leakage, gate-dielectric leakage and device to device variations. But FinFET based designs offers the better control over short channel effects, low leakage and better yield [13] below 45nm helps to overcome the obstacles in scaling. Double Gate devices have been used in a variety of innovative ways in digital and analog circuit designs. A parallel transistor pair consists of two transistors with their source and drain terminals tied together. In Double-Gate (DG) FinFETs, the second gate is added opposite to the traditional gate, which has been recognized for their potential to better control short channel effects, as well as to control leakage current. The operations of FinFETs is identified as Short Gate (SG) mode with transistor gates tied together, the Independent Gate (IG) mode where independent digital signals are used to drive the two device gates, the Low-Power (LP) mode where the back gate is tied to a reverse-bias voltage to reduce leakage power and the hybrid (IG/LP) mode, which employs a combination of low power and independent gate modes. Here independent control of front and back gate in DG FinFET can be effectively used to improve performance and
reduce power consumption. Independent gate control can be used to merge parallel transistors in non-critical paths[14].

Figure 1: Implementation of two gate FinFET

2.2 7T SRAM Cell Design Using FinFET

A SRAM cell is proficient of holding a data bit so long as the power is applied to the circuit. It consists of the central storage cell made up of two cross coupled inverters and two access transistors which provides read and write operation and the 7th transistor which is NMOS transistor is between the node and the driver transistor as shown in figure 2. The voltage dividing effect takes place at the inverter which stores '0', will be pulled up. In order to stop the transition, the 7th transistor at the other node is turned off so that the node which stores '1' will not be pulled down by the driver transistor as it acts a switch between the node and the driver transistor. The Conducting state of the access transistor is controlled by the control signal word line [12]. Whenever the word line is high, both access transistor conduct and provide the ability to write or read a data bit. When the word line is low, it isolates the storage cell. The access transistor connects the storage cell input/output nodes to the data lines which are complement to each other. In read operation, the bit lines start pre-charged to some reference voltage usually close to positive supply voltage [5].

In the standby mode the access transistors turn off by making the word line low [15]. The inverter will be complementary in this state. The PMOS of the left inverter is turned on, the output potential is high and the PMOS of the second inverter is switched off. The gates of the transistor that connect the bit line and the lines of the inverter are driven by the word line. If the word line is kept low the cell is disconnected from the bit lines. It has one additional transistor compared with standard 6T SRAM cell but operates more efficiently than 6T SRAM cell at low-VDD. The 7th transistor shown in figure 2 which is nMOS transistor is between the node and the driver transistor.

The voltage dividing effect takes place at the inverter which stores '0', will be pulled up. In order to stop this transition the 7th transistor at the other node is turned off so that the node which stores '1' will not be pulled down by the driver transistor as it acts a switch between the node and the driver transistor [16].

In the data retention period, the SRAM data will not be accessed. In this period, the wordline signal /WL is '1' and the nMOS transistor N5 is ON. In the read operation, the logical threshold voltage of the CMOS inverter driving node B increases when the data protection transistor N5 is turned OFF [7]. The FinFET designing parameters used in figure 2 are shown below

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Length</td>
<td>45nm</td>
</tr>
<tr>
<td>Width</td>
<td>120nm</td>
</tr>
<tr>
<td>Finger width</td>
<td>120nm</td>
</tr>
<tr>
<td>Source drain metal width</td>
<td>60nm</td>
</tr>
<tr>
<td>Drain diffusion area</td>
<td>16.8f</td>
</tr>
<tr>
<td>Source diffusion Area</td>
<td>16.8f</td>
</tr>
<tr>
<td>Drain Diffusion Periphery</td>
<td>520nm</td>
</tr>
<tr>
<td>Source Diffusion Periphery</td>
<td>520nm</td>
</tr>
<tr>
<td>Drain Diffusion res square</td>
<td>1.16667</td>
</tr>
<tr>
<td>Source Diffusion res square</td>
<td>1.16667</td>
</tr>
<tr>
<td>Left Source/Drain length (SA)</td>
<td>140nm</td>
</tr>
<tr>
<td>Right Source/Drain length (SB)</td>
<td>140nm</td>
</tr>
<tr>
<td>Gate Spacing (SD)</td>
<td>160nm</td>
</tr>
<tr>
<td>SCA</td>
<td>226.00151</td>
</tr>
<tr>
<td>SCB</td>
<td>0.11734</td>
</tr>
<tr>
<td>SCC</td>
<td>0.02767</td>
</tr>
</tbody>
</table>

2.3 Bit Finfet 7t Sram Cell

The 7T SRAM cell that stores one bit of information is shown in figure 2. The cell consists of two FinFET [6] inverters where the output of each is fed as input to other; this loop stabilized the inverters to their respective state. The access transistors and the Word Line (WL) and Bit Lines (BL) are used to write and read, to and from the cell. In the standby mode the access transistors turn off by making the word line low [15]. The inverter will be complementary in this state. The PMOS of the left inverter is turned on, the output potential is high and the PMOS of the second inverter is switched off. The gates of the transistor that connect the bit line and the lines of the inverter are driven by the word line. If the word line is kept low the cell is disconnected from the bit lines. It has one additional transistor compared with standard 6T SRAM cell but operates more efficiently than 6T SRAM cell at low-VDD. The 7th transistor shown in figure 2 which is nMOS transistor is between the node and the driver transistor.
3. Design Of 16-Bit 7t Sram Memory

This section describes the designing of 4x4 SRAM cell arrays of 4 rows and 4 columns. Each block of the array is of 7T SRAM cell. There are 4 rows and 4 columns arranged to form a 4x4 SRAM cell array. To address these rows of cells, the decoder is used prior to the array arrangement. As the row consists of 4 cells it constitutes to form half a byte. The AND based 2:4 decoder is used to generate the address lines, the number of transistors used for the decoder circuit is 28 (each AND gate uses 6 transistor and NOT gate made up of 2 transistors) [3]. These address lines which form the outputs of decoder are connected to each row of the array. The input and output data control consists of write and ready circuitry. From the decoder the address is selected in the array and 4 bits of data is written or read in parallel from cell 1 to cell 4. Input-output buffers are also required for each column as the decoder selects only one row of the array, the other cells may generate glitch, this can be nullified by the buffers.

Also a 8x1 Multiplexer can be used to combine all the output of single SRAM cells of each column to make a single output data. The figure 3 shows the 4x4 SRAM cell array design consists of 7T one bit SRAM cell, decoders and buffers. The total number of transistors utilized in this 4x4 SRAM cell array is 172[10].

3.1. Design Of 2:4 Decoder

A decoder is a digital logic circuit which takes multiple coded input and converts to coded multiple outputs where the input and output codes are different. The decoding is necessary in applications like data multiplexing, 7 Segment display and memory address decoding. The simple example of the decoder is an AND gate, the AND gate output will be high when all the inputs are high, this output is also known as active high output. A little more complex decoder is the n-2n binary decoders. These decoders convert n coded input to 2n unique outputs.

![Figure 3: Designed 4x4 SRAM cell array](image)

Also a 8x1 Multiplexer can be used to combine all the output of single SRAM cells of each column to make a single output data. The figure 3 shows the 4x4 SRAM cell array design consists of 7T one bit SRAM cell, decoders and buffers. The total number of transistors utilized in this 4x4 SRAM cell array is 172[10].

![Figure 4: 2:4 decoder designs using NOT and AND gate](image)

Figure 4 illustrates the decoder circuit for 2 coded inputs to 4 coded outputs. It consists of 2 NOT logic gates and 4 AND logic gates.

The output of the 2:4 decoders further clarified from its inputs like r1, r2 and outputs like WL1, WL2, and WL3 AND WL4. Figure 5 shows the inputs r1, r2 and corresponding outputs [8].

3.2. Read And Write Operation Of 4x Sram’s Cell Array

At initial stage of read operation, decoder will be in inactive mode. As soon as decoder is enabled, they are pre-charged first. This process makes all output high for a small amount of time. This address is invalid then address settles down according to the input of the decoder and one particular SRAM cell is activated. Activation of read enable (RE) signal activates the read buffer.

![Figure 5: 2:4 decoder simulation result](image)
The ready SRAM cell data traverses towards ready buffer. Thus the data bit is read from memory cell. To continue the read operation address bits are changed to address the next memory cell. During write operation, the address is selected and data is given to write circuit as input. Upon the activation of write enable (WE) signal activates the write buffer output change according to the input. The feedback action in SRAM cell then stabilizes the data of the memory. This signal is disabled for safe write operation and to avoid further writing of spurious data. To continue the write operation to other cells address bits are changed and same procedure is repeated again and again for required times. The figure 6 shows the simulated output of 4x4 SRAM cell array.

4. VARIABLE SUPPLY VOLTAGE SCHEME

Variable Supply-voltage is emerging as an effective technique for reducing both dynamic power and leakage power. Dynamic power is proportional to \( f \cdot C_{\text{LOAD}} \cdot V_{\text{DD}}^2 \), where \( f \) is the system clock frequency, \( C_{\text{LOAD}} \) is the effective load capacitance, and \( V_{\text{DD}} \) is the supply voltage. Scaling the supply voltage requires a commensurate reduction in clock frequency because signal propagation delays increase when the supply voltage is scaled down [11]. The maximum clock frequency at which a transistor can operate is proportional to \( V_{\text{DD}}^2 \), where \( V_T \) the transistor threshold voltage, and \( \alpha \) is strongly dependant on the mobility degradation of electrons in transistors (with typical value between 1 and 2). Therefore, variable supply-voltage can reduce dynamic power in the order of \( V_{\text{DD}}^2 \). As supply voltage scales down, the sub-threshold leakage and the leakage due to Drain Induced Barrier Lowering (DIBL) also decrease [9]. Hence, supply voltage scaling also helps in reducing leakage power. For 1.2 V, 0.13- \( \mu \)m technology, it is shown that the supply voltage scaling has impacts in the orders of \( V_{\text{DD}}^2 \) and \( V_{\text{DD}}^4 \) on sub-threshold leakage and gate leakage, respectively [1].

We consider a specific flavour of supply-voltage scaling, called Variable Supply-Voltage (Vs V) scaling, where we vary the supply voltage while a program executes. To ensure Vs effectiveness, we consider several circuit-level overhead issues. First, continuous voltage scaling can possibly achieve the best power savings, if we ignore the power and performance overhead due to the extra circuitry [17].

4.1. Effect On Leakage Current

The sub-threshold leakage is the drain-source current of a transistor operating in the weak inversion region. Contrasting the strong inversion region in which the drift current dominates, the sub-threshold conduction is due to the diffusion current of the minority carriers in the channel for a MOS device. The magnitude of the sub-threshold current is a function of the temperature, supply voltage, device size, and the process parameters out of which the threshold voltage (\( V_T \)) plays a dominant role [4].

In current CMOS technologies, the sub-threshold leakage current, \( I_{\text{SUB}} \), is much larger than the other leakage current components. This is mainly because of the relatively low \( V_T \) in modern CMOS devices. \( I_{\text{SUB}} \) is calculated by using the following formula:

\[
I_{\text{DS}} = K \left( 1 - e^{-\frac{V_{\text{DS}}}{V_T}} \right) e^{\frac{(V_{\text{GS}} - V_T + V_{\text{DS}})}{\eta V_T}}
\]

where \( K \) and \( n \) are functions of the technology, and \( \eta \) is the drain-induced barrier lowering coefficient. Figure 7 shows the comparative study of leakage currents at variable supply voltage. It clearly shows that FinFET array has small leakage current.

4.2. EFFECT ON DYNAMIC CURRENT

Estimation of dynamic current is important for several applications. Knowledge of the dynamic current consumption of an application can assist programmers in optimizing software for power consumption.
Power dissipation of the FinFET SRAM cell assesses the utility of the cell in portable devices. The fundamental advantage of the FinFET based SRAM is in its low access time and power dissipation due to low leakage current in FinFET device.

While a strong driving current reduces the access time, it also increases the power dissipation in the SRAM cell. However to reduce power dissipation, leakage currents need to be minimized which permit an increase in the channel length or higher transistor threshold voltages. Larger channel length results in higher delay and there exists a trade-off between these two performance indices [2]. Figure 8 shows the comparison of dynamic current of CMOS and FinFET SRAM array. It confirms that FinFET technology reduces power consumed by memory compared to CMOS.

### 4.3. EFFECT ON DELAY

We considered the operation speed of the FinFET SRAM and CMOS array as shown in Fig. 9. The read and write delays were extracted are function of the number of rows. It was found that the FinFET SRAM realized the read and write operations roughly twice faster than that of the bulk-planar one. The comparison in delay by giving variable supply voltage of CMOS and FinFET SRAM array is shown in Figure 9.

As supply voltage scales down, the sub-threshold leakage and the leakage due to Drain Induced Barrier Lowering (DIBL) also decrease. Hence, supply voltage scaling also helps in reducing leakage power.
6. Conclusion

In this paper, FinFET based 7T SRAM has been designed and analysis have been carried out for leakage current, dynamic power and delay. Furthermore, 2:4 decoder has been designed and results obtained through proposed model have been verified. Once all sub-blocks such as 1-Bit 7T SRAM and 2:4 decoder have been designed using FinFET device, then all the sub blocks is integrated and 4x4 SRAM cell array has been developed. For the validation of our design approach of 7T SRAM, output of FinFET SRAM array have been compared with standard CMOS SRAM and significant improvements are achieved in proposed model. Mixed results are achieved at the point of leakage current and Dynamic Current. For minimum consumption, devices are operated at 0.6V and for Minimum delay, devices are operated at 0.9V. So supply voltage is so chosen according to the requirement of the application.

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Reference


<table>
<thead>
<tr>
<th>Parameter</th>
<th>FinFET 16 bit SRAM array</th>
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<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>0.6 0.7 0.8 0.9 1</td>
</tr>
<tr>
<td>Leakage Current (nA)</td>
<td>28.66 39.39 44.64 37.52 36.88</td>
</tr>
<tr>
<td>Leakage Power (fW)</td>
<td>279.6 368.7 74.86 221.5 340.1</td>
</tr>
<tr>
<td>Dynamic Current</td>
<td>2.21 8.46 16.02 26.2 37.02</td>
</tr>
<tr>
<td>Dynamic Power</td>
<td>34.02 313.3 630.5 1.05 1.29</td>
</tr>
<tr>
<td>Delay (write ps)</td>
<td>200.2 188.3 174.5 182.1 193.7</td>
</tr>
<tr>
<td>Delay (read ps)</td>
<td>425.8 254.2 229.6 224.2 229.0</td>
</tr>
</tbody>
</table>

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